

1 **WHAT IS CLAIMED IS:**

2 1. A parallel redundant power system composed of plural UPS modules
3 each of which having an inverter, wherein an AC output of each inverter is
4 coupled to a load through a bus for collectively supplying a load current, wherein
5 the plural UPS modules are connected in parallel via a current sharing circuit, a
6 synchronizing clock signal circuit and a communication circuit coupled among
7 the UPS modules,

8 wherein the synchronizing clock signal circuit controls the phases of all
9 output voltages of the inverters to be synchronal to each other;

10 wherein the current sharing circuit controls the current rate that each
11 UPS module should output, and furthermore by properly controlling unbalance
12 power among the USP modules to mitigate the cross current among the UPS
13 modules; and

14 wherein the communication circuit is used to control information
15 exchange among the parallel UPS modules.

16 2. A parallel redundant power system composed of plural inverters,
17 wherein an AC output of each inverter is coupled to a load through a bus for
18 collectively supplying a load current, wherein the plural inverters are connected
19 in parallel via a current sharing circuit, a synchronizing clock signal circuit and a
20 communication circuit coupled among the inverters,

21 wherein the synchronizing clock signal circuit controls the phases of all
22 output voltages of the inverters to be synchronal to each other;

23 wherein the current sharing circuit controls a rate of current that each
24 inverter should output, and furthermore by properly controlling unbalance power

1 among the USP modules to mitigate the cross current among the inverters; and
2 wherein the communication circuit is used to control information
3 exchange among the plural parallel inverters.

4 3. The power system as claimed in claim 1, wherein the synchronizing
5 clock signal to control the plural inverters is an internal synchronizing signal.

6 4. The power system as claimed in claim 2, wherein the synchronizing
7 clock signal to control the plural inverters is an internal synchronizing signal.

8 5. The power system as claimed in claim 1, wherein the synchronizing
9 clock signal to control the plural inverters is generated by one of the parallel
10 inverters .

11 6. The power system as claimed in claim2, wherein the synchronizing
12 clock signal to control the plural inverters is generated by one of the parallel
13 inverters.

14 7. The power system as claimed in claim 1, wherein the current sharing
15 circuit controls all plural inverters to equally share the load current based on the
16 quantity of the plural inverters.

17 8. The power system as claimed in claim 2, wherein the current sharing
18 circuit controls all plural inverters to equally share the load current based on the
19 quantity of the plural inverters.

20 9. The power system as claimed in claim 1, wherein the current sharing
21 circuit controls all inverters, which has the same rating capacities, to share the
22 load current with different current sharing ratio.

23 10. The power system as claimed in claim 2, wherein the current sharing
24 circuit controls all inverters, which has the same rating capacities, to share the

1 load current with different current sharing ratio.

2 11. The power system as claimed in claim 1, wherein the plural inverters
3 with different rating capacities are coupled in parallel and share the load current
4 based on ratio commands of the current sharing circuit, wherein each ratio
5 command is independent to the others.

6 12. The power system as claimed in claim 2, wherein the plural inverters
7 with different rating capacities are coupled in parallel and share the load current
8 based on ratio commands of the current sharing circuit, wherein each ratio
9 command is independent to the others.

10 13. The power system as claimed in claim 1, wherein each inverter
11 further comprises a switch element, and when the switch element is switched off,
12 the inverter is isolated from the other inverters and operated independently to
13 supply power to the load.

14 14. The power system as claimed in claim 2, wherein each inverter
15 further comprises a switch element, and when the switch element is switched off,
16 the corresponding inverter is isolated from the other inverters and operated
17 independently to supply power to the load.

18 15. The power system as claimed in claim 1, wherein each inverter
19 further comprises a digital signal processor (DSP) to control the current sharing
20 circuit, the synchronizing clock signal circuit and the communication circuit.

21 16. The power system as claimed in claim 2, wherein each inverter
22 further comprises a digital signal processor (DSP) to control the current sharing
23 circuit, the synchronizing clock signal circuit and the communication circuit.

24 17. The power system as claimed in claim 15, the DSP storing a quick-

1 speed control software for transient control of the power system, wherein the
2 quick-speed control software detects a direct current (DC) voltage of the bus, the
3 output voltage value and the output current value of each inverter, wherein
4 during at least one switching cycle, the rapid control software calculates an
5 inverter current command and a current sharing command to control a pulse
6 width modulation (PWM) signal applied to each inverter.

7 18. The power system as claimed in claim 16, the DSP storing a quick-
8 speed control software for transient control of the power system, wherein the
9 quick-speed control software detects a direct current (DC) voltage of the bus, the
10 output voltage value and the output current value of each inverter, wherein
11 during at least one switching cycle, the rapid control software calculates an
12 inverter current command and a current sharing command to control a pulse
13 width modulation (PWM) signal applied to each inverter.

14 19. The power system as claimed in claim 15, the DSP storing a low-
15 speed control software for static control of the power system, wherein the low-
16 speed control software utilizes calculation of an unbalanced power parameter
17 based on the detected output impedance, the phase difference and voltage
18 difference through the current sharing circuit, further, the low-speed control
19 software adjusts the cross current once per at least one output voltage cycle.

20 20. The power system as claimed in claim 16, the DSP storing a low-
21 speed control software for static control of the power system, wherein the low-
22 speed control software utilizes calculation of an unbalanced power parameter
23 based on the detected output impedance, the phase difference and voltage
24 difference through the current sharing circuit, further, the low-speed control

1 software adjusts the cross current once per at least one output voltage cycle.

2 21. The power system as claimed in claim 15, wherein the DSP is
3 provided to perform the transient control and the static control of the power
4 system, wherein the control gain values of the transient control and the static
5 control are adjustable.

6 22. The power system as claimed in claim 16, wherein the DSP is
7 provided to perform the transient control and the static control of the power
8 system, wherein the control gain values of the transient control and the static
9 control are adjustable.

10 23. The power system as claimed in claim 1, wherein the inverter is an
11 output inverter of the UPS module.

12 24. The power system as claimed in claim 1, wherein there are three
13 phases of the output voltage and at least one of the three phases is controlled to
14 be phase locked.

15 25. The power system as claimed in claim 2, wherein there are three
16 phases of the output voltage and at least one of the three phases is controlled to
17 be phase locked.

18 26. A load sharing control method by using an unbalanced power to
19 adjust active power, the method applying for a power system composed of at
20 least two inverters coupled in parallel to provide AC power to a load through a
21 bus, the method comprising the steps of:

22 sampling an output voltage $v_o(t)$, a load current $i_{load}(t)$, and a current
23 sharing command $i_{load}^*(t)$ generated from a current sharing circuit;

1 calculating a difference value $i_e(t)$ by comparing the sampled load
2 current with the sampled current sharing command, wherein the difference value
3 is expressed by $i_e(t) = i_{load}^*(t) - i_{load}(t)$;
4 integrating the product of the difference value $i_e(t)$ and the output
5 voltage $v_o(t)$ during an output voltage cycle T, and then calculating an
6 unbalanced power P_{unbal} according to an equation $P_{unbal} = \frac{1}{T} \int i_e(t) \times v_o(t) dt$; and
7 adjusting the output voltage $v_o(t)$ of the inverter based on the unbalanced
8 power.

9 27. The method as claimed in claim 26 further comprising the steps of:

10 establishing a relationship between the unbalanced power P_{unbal} and a
11 reference voltage V_{ref} , wherein the relationship is expressed by an equation

$$12 \quad V_{ref} = V_{setting} + K_1 \times P_{unbal};$$

13 wherein $V_{setting}$ is a preset initial voltage of the reference voltage V_{ref}
14 and K_1 is a gain value that is inversely proportional to the difference value $i_e(t)$.

15 28. The method as claimed in claim 27, wherein the unbalanced power is
16 generated when the amplitude of the output voltages, the output impedance, or
17 the phases of the output voltages of the at least two inverters are different to each
18 other.

19 29. A load sharing control method for adjusting active power, the
20 method applying for a power system composed of at least two inverters coupled
21 in parallel to provide AC power to a load through a bus, the method comprising

1 the steps of:

2 detecting a DC bus voltage $V_{realBUS}$;

3 comparing the detected DC bus voltage $V_{realBUS}$ with a preset DC bus

4 voltage $V_{BUSsetting}$ to obtain a difference value ΔV_{BUS} , where the difference value

5 is expressed by $\Delta V_{BUS} = V_{realBUS} - V_{BUSsetting}$;

6 establishing a relationship between the difference value ΔV_{BUS} and a

7 reference voltage V_{ref} , where the relationship is expressed by an equation

8 $V_{ref} = V_{setting} + K_2 \times \Delta V_{BUS}$, wherein $V_{setting}$ is a preset initial voltage of the

9 reference voltage V_{ref} and K_2 is a gain value.

10 30. The method as claimed in claim 29, wherein the gain value is
11 inversely proportional to the current sharing difference.

12 31. A load sharing control method by using a current sharing error to
13 adjust a transient current of a power system composed of at least two inverters
14 coupled in parallel so as to provide AC power to a load through a bus, the method
15 comprising the steps of:

16 sampling a load current $i_{load}(t)$ and a current sharing command $i_{avg}(t)$

17 generated from a current sharing circuit;

18 comparing the sampled load current $i_{load}(t)$ and the current sharing

19 command $i_{avg}(t)$ to obtain a current sharing difference and then multiplying the

20 current sharing difference by a gain value K_{i2} to derive a compensation

21 command $i_{com}(t)$, where the compensation command is expressed by an

1 equation $i_{com}(t) = K_{i2} * (i_{avg}(t) - i_{load}(t))$; and

2 applying the compensation command $i_{com}(t)$ to adjust the load current

3 $i_{load}(t)$.

4 32. The method as claimed in claim 31, wherein the gain value K_{i2} is

5 inversely proportional to the current sharing difference.

6 33. A method for protecting a power system composed of at least two

7 inverters coupled in parallel so as to provide AC power to a load through a bus,

8 the method comprising the steps of:

9 sampling an output voltage v_k and an output current i_k during a period N ;

10 calculating an active power P_{NEG} , wherein the active power is calculated

11 according to an equation $P_{NEG} = (\sum_{k=0}^N v_{pk} i_{pk}) / N$;

12 determining whether the active power is a negative value, if the active

13 power is a negative value and smaller than a preset negative limit value, then

14 isolating the one of the at least two inverters from other inverter.